An Autonomous SRAM With On-Chip Sensors in an 80-nm Double Stacked Cell Technology

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Abstract—An active solution is proposed to overcome the uncertainty and fluctuation of the device parameters in nanotechnology SRAM. The proposed scheme is composed of sensing blocks, analysis blocks and control blocks. An on-chip timer, temperature sensor, substrate noise detector, and leakage current monitor are used to monitor internal status of chip during operation. From the sensed data, internal supply voltage, internal timing margin from decoding to sensing time, substrate noise from digital area, and low voltage level of wordline are controlled. A 512-kb test SRAM chip, fabricated with an 80-nm double stacked cell technology, shows that average power consumption is reduced by 9% and the standard deviation decreases by 58%.

Index Terms—Leakage current monitor, on-chip timer, SRAM, substrate noise, temperature sensor.

I. INTRODUCTION

Fig. 1. S^3 SRAM cell vertical structure [3].

RECENTLY, with the rapid advance of the silicon process technology, SRAM has met several severe problems. Density limitation due to relatively large cell size, increased leakage current arising from higher density, static noise margin of cell, and soft error rate from small cell node capacitance are major concerns for SRAM engineers [1], [2].

Especially, the density limitation is the most urgent problem to SRAM as a standalone memory. For fast access speed, the embedded SRAM is used rather than the standalone SRAM due to the off-chip bandwidth limitation. Furthermore, the operating speed of DRAM becomes fast comparable to SRAM by using various circuit techniques and process technology. Even in mobile applications, the mobile DRAM has been widely adopted due to its low cost and high density.

To enhance the density limitation of SRAM, stacked single-crystal silicon (S^3) SRAM cell technology was introduced [3]. This technology achieves 0.16-μm^2 cell size by stacking transistors twofold as shown in Fig. 1. This is one third of the size of the conventional SRAM cell, and only 2.9 times that of a DRAM cell in the same technology.

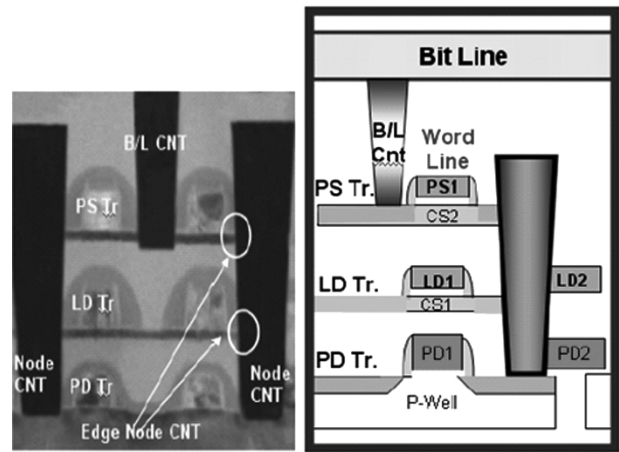On the other hand, as the technology scaling progresses, the transistor size becomes small and the SRAM's capacity becomes higher than before. At the same time, the distribution of the device parameters from chip to chip and from wafer to wafer becomes wider as shown in Fig. 2. A conventional approach to overcome uncertainties is the statistical design methodology, which is based on the prediction of the variation of device parameters. However, it is very difficult to get detailed information about the statistical variation of the device parameters during operation and the SRAM product suffers from performance losses because it must be designed with consideration of the worst case conditions and parameters. Since S^3 SRAM integrates double-folded cell structure with six transistors in only 0.16 μm^2, the influence of process, voltage, and temperature (PVT) variations on the cell's features is greater than the cases of other types of cells. Contrary to the previous statistical approach during design stage, we propose a new method—fine tuning of the internal conditions after fabrication. Active control of the operating conditions by using sensing, analysis, and control (SAC) after fabrication can enhance the yield of SRAM based on the measured real parameter values. Fig. 3 shows the concept of the scheme. In this paper, SAC and its application to S^3 SRAM will be explained to alleviate PVT dependency for high yield of high-density SRAM.

The paper is organized as follows. Section II describes an overview of the proposed scheme, SAC. Section III describes the key blocks of the SAC in detail. SAC is composed of an on-chip timer, a temperature sensor, a substrate noise manager, and a leakage current monitor. Section IV presents the implementation results of the test chip. Concluding remarks are made in Section V.
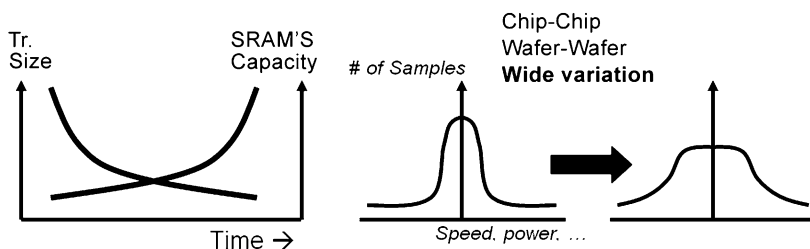
Fig. 2. Trends of SRAM according to technology evolution.
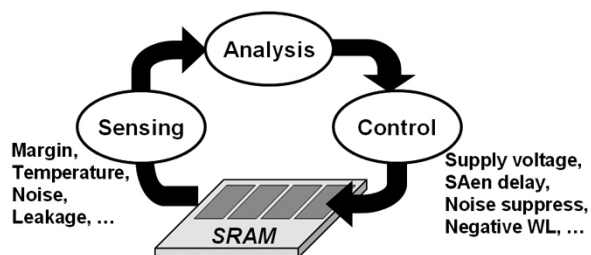
Fig. 3. Concept of the proposed SAC scheme.

(a)

Sensor	Analysis	Control	Effect
On-Chip Timer	> Margin	iVdd	Low power
Temp. Sensor	50C, 100C	SAen delay	Wide margin
Substrate Noise Detector	> 150mV	Active decoupling	Silent Sub.
Leakage Current Monitor	> 1μA/blk	Negative wordline	Low power

(b)

Fig. 4. Proposed SAC scheme. (a) Block diagram. (b) Summary table.

II. SENSING, ANALYSIS, AND CONTROL

Careful and detailed control of the device features is necessary and more precise data on the conditions under which the device operates are required for stable operation of deep-sub-micron CMOS devices. Various active control methods such as dynamic voltage and frequency scaling have been studied actively [4]–[6], and have been applied to microprocessors and embedded system, where these methods are relatively easy to apply. However, the operation voltage range of the memory cell array is not as wide as that of digital logic circuits, preventing dynamic voltage scaling methods from being applied to memory [7]. In memory products, as a passive method, a voltage control of the cell array was performed according to active and standby modes in order to reduce their power consumption in standby mode. But, as device technology shrinks and memory density goes up, an active control of the device parameters is also required in memory. That is because the application of conventional control methods to achieve stable operation without performance penalty has reached its limit for countering the increasing fluctuation and uncertainty of device parameters.

In this paper, as an active control method, the SAC scheme is introduced to SRAM. SAC is composed of three steps: sensing the internal status of chip by on-chip sensors, analyzing data from sensors by decision logic, and controlling the parameters for stable and desirable operation. Fig. 4(a) shows the block diagram of the proposed SRAM with SAC. In addition to the conventional SRAM circuits, measurement blocks, diagnostic blocks, and controller blocks are added as described in the gray blocks.

First, the on-chip timer receives signals from the control box and data-latch. The timing margin is measured and the result is used to control the internal $V_{\rm dd}$ level. Second, the temperature sensor measures on-chip temperature during operation. Sense-amplifier-enable delay (SAen), the delay from the rising edge of wordline to the enable time of the sense amplifier, is

modified by the measured data. SNM, the substrate noise manager, is located in the boundary between the digital and analog areas. "Analog area" means the cell core block including the sense amplifier and cell array. SNM is used for suppressing substrate noise from the digital area to analog blocks. Finally, LCM, the leakage current monitor, measures the current of each cell array block on standby mode. Based on the data, the low level of the wordline is set to zero or to negative voltage by the negative voltage generator (NVG), reducing the leakage current from unselected rows.

Fig. 4(b) shows the parameters used for the SAC scheme. Among various device parameters, we choose read cycle time margin, on-chip temperature, substrate noise, and leakage current, which are measured by various on-chip sensors. The on-chip timer is used to check read cycle timing margin. According to the measured value of the timing margin, the internal $V_{\rm dd}$ level is varied to modify it. An on-chip temperature is measured by the temperature sensor and SAen delay is controlled at 50 °C and 100 °C. Its basic purpose is to widen the timing margin, and, in addition, to improve the speed. When substrate
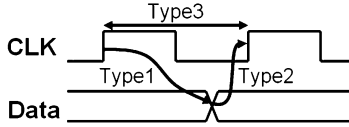
Fig. 5. Measurement points of the on-chip timer.

noise level is over 150 mV, the SNM suppresses the substrate noise by active decoupling method. The leakage current monitor is to check whether the leakage current of each cell array block is over 1 μA. When excessive leakage current is detected, a negative voltage signal is applied to the unselected rows to reduce leakage current for low power consumption can be achieved by appropriate negative voltage generator operation.

III. KEY BUILDING BLOCKS

A. On-Chip Timer

Although lowering supply voltage is a very effective way to reduce power consumption, it can cause problems in the cycle time and static noise margin of the SRAM cell. Hence, the on-chip timer is adopted to check the cycle time margin.

A small-size SRAM cell like the S^3 SRAM cell cannot generate enough cell current for bitline swing so that the read cycle timing margin becomes the limitation of the cycle-time. The on-chip timer measures three types of delays as shown in Fig. 5: from clock rising edge to data transition in data latches (Type 1), from the data transition to the next clock rising edge (Type 2), and from clock to next clock (Type 3). Type 1 measures the critical path of read cycle, while type 2 measures the timing margin of read cycle. In addition, to convert the measured number to real time data, type 3 is necessary. Type 1 and 3 can be used in wafer level test and is especially effective for the known-good-die test. Type 2 is used to control internal V_{dd} during operation. The test mode selection signal can switch the measurement type.

Fig. 6 shows the block diagram of the on-chip timer. CLKhigh is the pulse signal from the rising edge of the clock signal. DATAtran is the pulse signal from the data latch. OSCen is enabled by rising edge of CLKhigh and disabled by DATAtran rising edge. With OSCen high, a ring oscillator in Clock Gen generates pulse stream of CLKcoarse. CLKfine is the next clock pulse after CLKcoarse is disabled. From these signals, MSB 8 bits are generated by the 8-bit synchronous counter and LSB 4 bits by the fine delay measure unit.

Fig. 7 shows the signal waveforms of the on-chip timer. The OSCen enables the ring oscillator to make CLKcoarse signal. The upper 8 bits of the timer are made by CLKcoarse. If N clocks are counted, the coarse delay is $N-1$. The lower 4 bits denote the fine delay. The fine delay measurement block is composed of a 16-stage inverter chain and 16 D-flip-flops. The propagation stages from FMstart to CLKfine determine m, and then 16-m is the actual value of the fine delay.

The resolution of the delay measurement is two inverter-delays of a typical-size MOSFET. In the test SRAM, it is ~0.2 ns at 1.6 V of the internal V_{dd}, which is enough to represent the cycle time margin.
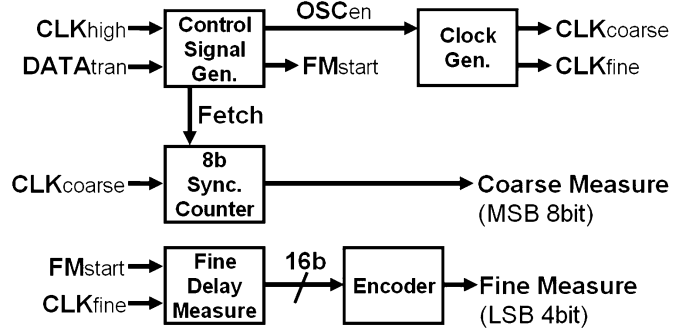

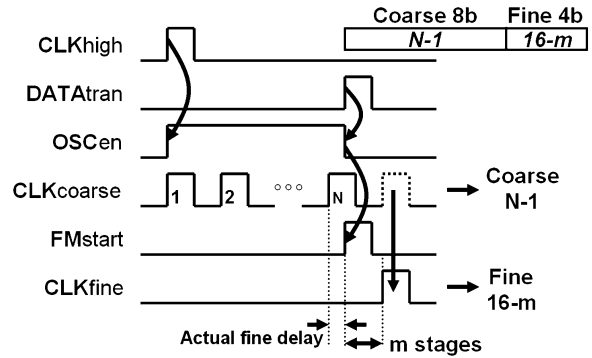Fig. 6. Block diagram of the on-chip timer.

Fig. 7. Waveform of the on-chip timer.

According to the values of the on-chip timer, the internal supply voltage level is controlled for low-power consumption and stable operation. When enough margins exist, internal supply voltage is dropped until it reaches the pre-defined voltage level given by the data retention voltage of the SRAM cell, which is about 0.8-V. In addition, the internal voltage can be lowered as long as the value of on-chip timer has a finite operation margin. On the contrary, when the cycle time margin is insufficient, the internal supply voltage should be raised for more stable operation.

The way to measure the read cycle timing margin depends on the SRAM's operation mode [8]. For the flow-through mode, the SRAM can output read data in one cycle. But, in pipelined mode, the timing margin is set to negative value. The test SRAM is designed to use the flow-through mode.

B. Temperature Sensor

In memory products, an on-chip temperature sensor has been seldom integrated so far. Recently, it is used for controlling the self-refresh period automatically in mobile DRAM products [9].

In SRAM, one important factor to affect read cycle time is the sense-amplifier-enable delay (SAen delay). SAen delay is equal to an additional delay time inserted between the wordline enable time and sense-amplifier-enable time. In general, SRAM has an option to modify the delay during the test time because the performance of the cell and the core circuit is unknown before fabrication and the final tuning is necessary for the optimum operation according to the measured value after fabrication. The proposed SRAM can adjust the SAen delay with eight steps of 2-ns delay elements at 1.6-V internal V_{dd}. Since the delay circuit
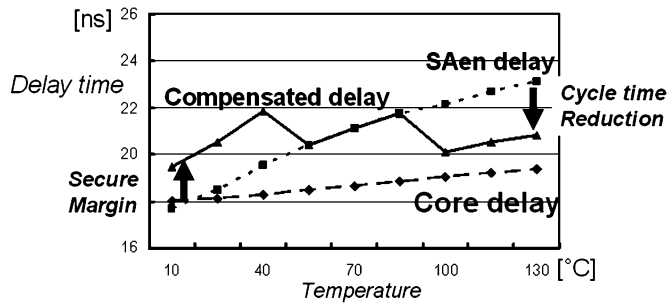
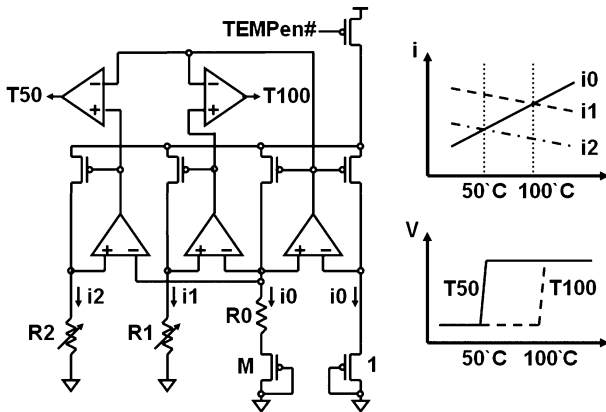Fig. 8. Core delay versus SAen delay versus compensated delay.

Fig. 9. Temperature sensor.

for the SAen generation uses relatively long channel length transistors in order to make long delay, it suffers from the voltage and temperature variations. Especially, the temperature has different effects on the core delay and the SAen delay. The core delay means the delay from the wordline rising edge to the time when the bitline pair develops enough voltage difference, about 50 mV. The core delay is composed of the decoding delay time and the bitline-evaluation time.

As temperature varies, the core delay and the SAen delay behave differently, because the decoding delay time is made of the propagation delay of the transistors with short channel length and the bitline-evaluation time is mainly the RC time constant of the bitline metal capacitance. These two components are relatively insensitive to temperature variation compared with transistors with long channel length. As shown in Fig. 8, without thermal compensation, SAen delay increases at high temperature not suitable for high-speed operation, and at low temperature, SAen delay decreases, losing operational margin. To overcome this temperature dependence, the modification of SAen delay time according to temperature variation is necessary, securing the timing margin at cold temperature conditions and reducing cycle time at hot temperature conditions.

Compensation is performed by the output signals, T50 and T100, of the temperature sensor as shown in Fig. 9. T50 and T100 are signals representing the boundary of $50\,^{\circ}C$ and $100\,^{\circ}C$, respectively.

The architecture of the circuits in Fig. 9 is based on the low-voltage bandgap reference circuit. Output signals can be obtained by the difference in the temperature dependency of each

current. For the compensation of process variation, the values of R1 and R2 can be measured by test signals and modified by fuse blowing. According to the combination of signals T50 and T100, the SAen delay is adjusted. If the temperature is higher than $100\,^{\circ}C$, SAen delay is reduced to give the SRAM more margins in cycle-time. This can lower internal supply voltage for low-power consumption. On the contrary, if it is lower than $50\,^{\circ}C$, SAen delay is increased by one step to stabilize the read operation.

C. Substrate Noise Manager (SNM)

Recently, the effects of the substrate noise from digital circuits to analog circuits have been studied actively [10]–[12]. As the access speed of the SRAM is raised more and more, the effect of the substrate noise from control and decoding circuits to cells can not be ignored. So we propose substrate noise manager (SNM) composed of substrate noise detector (SND) and substrate noise suppressor (SNS). These two components are combined to suppress noise for stable core operation or stable operation at lower V_{dd}. In addition, this results in low power consumption finally.

Fig. 10(a) shows the schematic diagram of the SND circuits. If the substrate noise is low, the voltage level of the gate of nMOS M1 is near ground and the node VC3 remains high. Otherwise, the gate signal of nMOS M1 oscillates according to the noise and the charge at the node VC3 is discharged gradually. In this way, the SND integrates substrate noise in pre-determined period, and asserts the signal NOISY when the integration voltage level at the node VC3 is under the logic threshold voltage of the inverter as shown in Fig. 10(b). Sensitivity of the SND can be controlled by the resistor R3 and the period of signal PRECH#. The active decoupling circuit SNS of Fig. 11(a) is activated by the signal NOISY from SND and suppresses substrate noise level low. By suppressing substrate noise, the operation of the analog circuits like sense amplifier can be stabilized with shorter SAen delay time. The silent grounds of Fig. 10 and Fig. 11 are made by using independent ground pads. These grounds are not used except for the SND and the SNS so that the influence of the operation of internal digital logic is reduced.

SRAM can secure more cycle-time margin and can lower operating-supply-voltage as well. Fig. 11(b) shows the frequency response of the SNS. It has 22-dB gain and 870-MHz gain bandwidth. The SNS effectively suppresses the substrate noise from 10 to 500 MHz, which covers the range of the operating frequency of the circuits inside SRAM. Fig. 12 shows the simulation results of the operation of the SNM. With the help of SNM, the peak-to-peak voltage of substrate noise is reduced by 45%, from 220 to 120 mV.

D. Leakage Current Monitor (LCM)

Recent research has reported many ways to reduce the leakage current of SRAM cells [13]–[16]. Although the cell data of SRAM is always maintained with the application of the power supply, cell leakage causes sizable standby current. As the density of SRAM becomes greater, the leakage current problem becomes very significant. The most frequently used way to solve the problem is to use dual-Vt transistors in cell [13], [14]. Other popular methods are to use the gated-ground
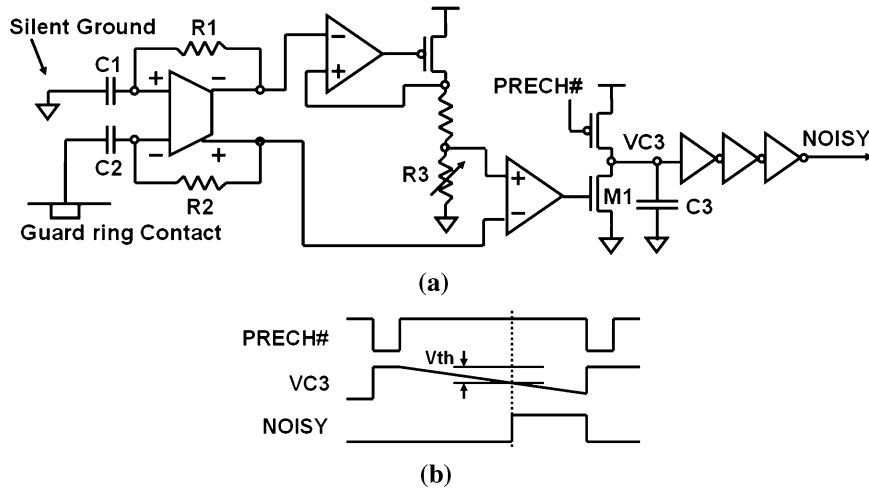
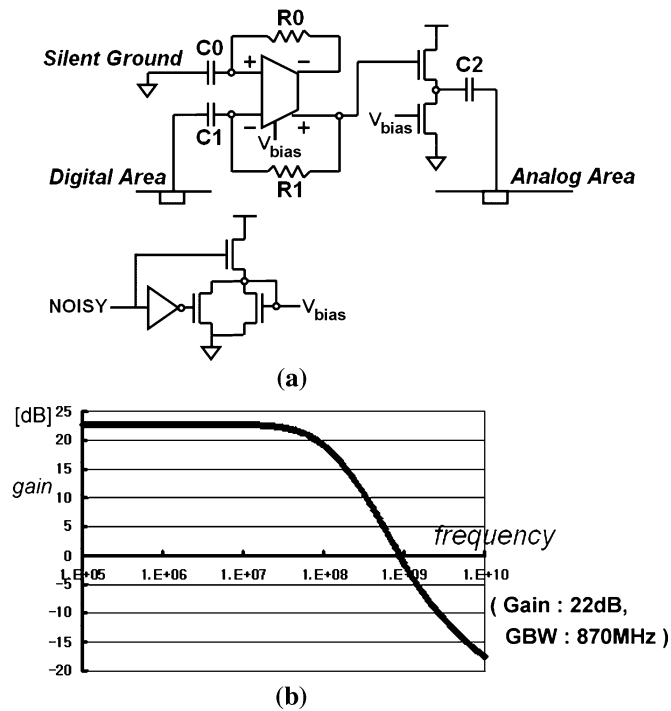Fig. 10. (a) Schematic and (b) waveform of substrate noise detector.

Fig. 11. (a) Schematic and (b) frequency response of substrate noise suppressor.

Fig. 12. Simulation results of substrate noise manager.
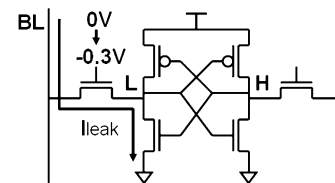
Fig. 13. Leakage current path of SRAM cell.

method or to control the supply voltage level of cell array according to operating mode [15], [16]. However, the first method needs additional process support and the second method controls the power supply of the cell core directly. In our test SRAM, the low voltage level of the wordline is controlled to reduce leakage current. The greatest difference between our scheme and the previous works is whether or not the internal status of SRAM is taken into consideration.

The basic purpose of the LCM is to monitor the leakage current of each cell array block. If the leakage current exceeds the predefined level, the low voltage level of the wordline is lowered to -0.3 V to reduce leakage current. Especially, the current from the bitline precharge transistor to the pull-down transistor is suppressed as shown in Fig. 13. On the contrary, if the leakage current is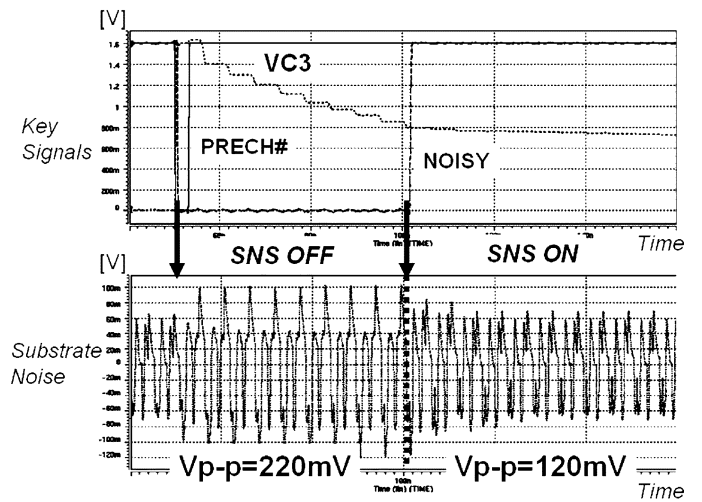 under the required level, negative voltage generator is disabled to save additional power consumption. -0.3-V is found as the optimum voltage to suppress leakage in this process. However, lower voltage than -0.3-V can cause reliability problems.

Fig. 14 shows the schematic diagram of LCM. In normal operation, LCM is turned off and power supply voltage is provided to the cell core through M1 and M2. In test mode, CPEN# is switched to high and LCM is activated. The cell current i_{leak} is replicated by m4 and the Vsen is generated by R1 and i_{leak}. When the Vsen is higher than the pre-defined value of Vlkg signal, LGK0 is turned on. The LKG0 is the enable signal for negative voltage generator (NVG) and determines the low level of the wordline. The source and bulk voltage of the pull-down transistor of the final row decoders are made to negative voltage
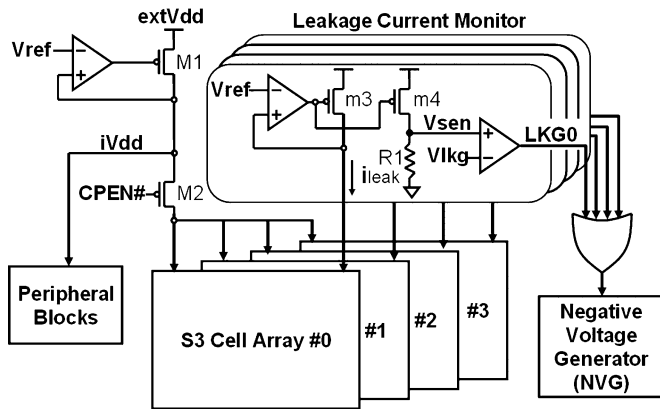
Fig. 14. Leakage current monitor.

by the NVG, and the low level of the wordline voltage falls down to about -0.3 V. In this way, the proposed scheme does not affect the cell array with small leakage current, but does affect the one with large leakage current.

Unlike other sensing blocks, LCM is activated in test mode or initialization mode because LCM consumes 82 μW which is larger than leakage current of cell array at external 3.3 V. The power consumption can be reduced by disabling NVGs as a result of LCM if its operation is not required. In addition, LCM is also efficient for the known-good-die test.

IV. IMPLEMENTATION AND TESTING

Fig. 15 shows the 512-kb test SRAM chip in an 80-nm double stacked S^3 SRAM cell technology with 3.3-V external and 1.6-V internal supply voltage. The chip area is 1152 μm $\times$ 1728 μm. The SNM is located between the cell array and other peripheral circuits. The cell array is composed of four 128-kb blocks. The LCM monitors each cell current of the cell array block. The delay control block of Fig. 4 is included in Ctrl Box. In a high-density SRAM product, it is difficult to find the boundary of the digital and analog areas. In that case, the position of SNM must be located near the control and pre-decoding blocks which are the potential substrate noise generator. The total of the area of all SAC components is 215 100 μm^2 and the sizes of the temperature sensor and the SNM are 9100 μm^2 and 20 400 μm^2, respectively. In a high-capacity SRAM, two temperature sensors are enough to control SAen delay because only the rough measurement results like cold, middle, and hot temperature are applied to the SAen delay controller. Also, two or four SNMs are enough to effectively suppress substrate noise from digital logic because they are located at the boundary of centered digital logic. Assuming that two temperature sensors and four SNMs are used in a 10-mm $\times$ 10-mm large SRAM, the area impact of the SAC circuit is about 0.3%.

Fig. 16 shows the test results of the proposed SRAM with and without SAC at room temperature. Forty samples from various wafers and lots were tested. The most remarkable change was the reduction of the distribution of power consumption to about one half. The average power consumption was reduced by 9% from 15.9 to 14.4 mW. Maximum power consumption was also reduced by 17% from 20.5 to 17.1 mW. More importantly, the standard deviation of power consumption was reduced significantly by 58% from 2.6 to 1.1 mW. From these results, it is
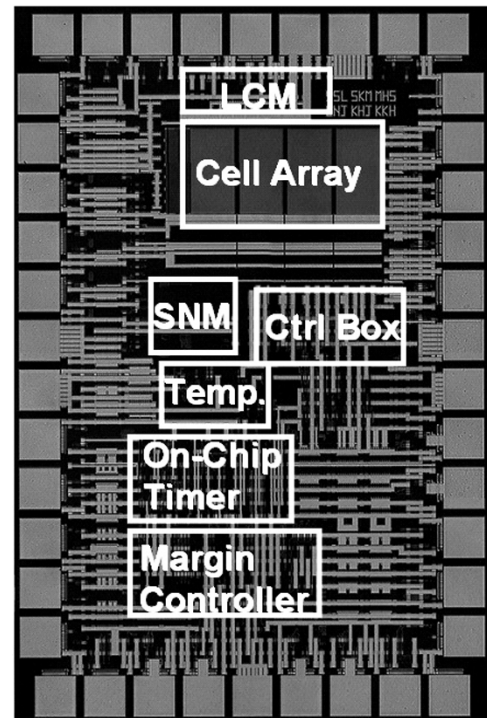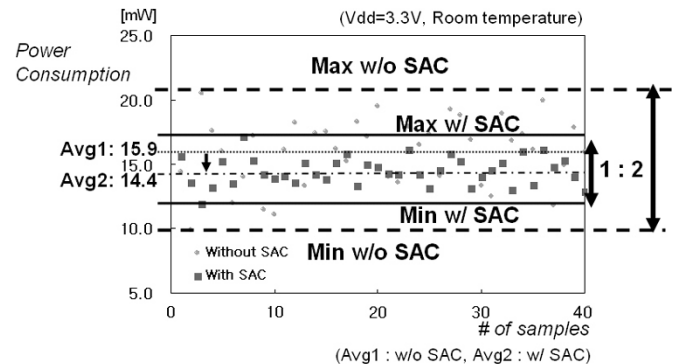

Fig. 15. Die photograph.

Fig. 16. Measured power consumption with SAC and without SAC.

clear that the implemented SRAM reduces not only its power consumption but also chip-to-chip variation by using the proposed SAC scheme.

The impact of each SAC circuit on power consumption is as follows. At first, the on-chip timer is the most effective component to reduce the power consumption. The internal V_{dd} level is controlled by the measurement results of the on-chip timer. The activation of the on-chip timer decreases the power consumption by 12%. The temperature sensor does not affect the average power consumption of the test chips because the chips were tested at the room temperature. The major role of the temperature sensor is to secure wide timing margin and stable operation as temperature varies. The power consumption overhead of the temperature sensor is 0.4%. In case of the SNM, on the contrary, the power consumption is raised in some samples because the SNS is activated when substrate noise is detected. The SNM is also focused on the stable operation rather than the reduction of the power consumption. The use of the SNM increases the
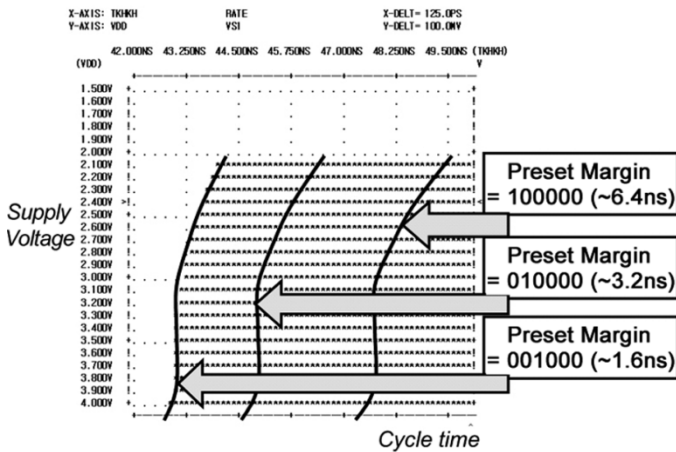
Fig. 17. Cycle time shmoo according to the preset margin.

average power consumption of the test chips by 5.2%. Finally, the LCM reduces the average power consumption by 3%, due to disabling the NVG when the LCM detects the cell leakage current below the desired value.

Fig. 17 shows the cycle time shmoo according to a preset read timing margin. The smaller the preset read timing margin is the larger a maximum operation frequency. If the preset margin is set to $100000_{(2)}$, the maximum operation frequency is 20.8 MHz. In case of $001000_{(2)}$, the maximum operation frequency is increased to 23.2 MHz. At the same cycle time, if the read timing margin is set to a small value, power consumption is also decreased by lowering internal supply voltage. However, in an extreme case, read operation cannot be performed normally. Thus, determining proper read timing margin is crucial and initial tests must be executed many times.

The operation speed of memory product is decided at hot temperature condition. So, the cycle time is reduced by about 2 ns when the temperature sensor is activated. This mechanism was explained in Section III-B and the function was confirmed by chip test.

The use of the SNM can make substrate noise low and the operation of the sense amplifier stable. Especially, the sense amplifiers operate stably even without large timing margin due to reduced substrate noise. For example, eight of 40 samples operate well with one-step reduced SAen delay, which means that its timing margin can be reduced by 2 ns.

All component circuits of the SAC scheme are designed to be turned on and off independently. The effect of the on-chip timer to the power consumption is the greatest among all component blocks of the SAC.

The power consumption overhead of the SAC scheme is under 8% at test chip. In high-density SRAM products, the overhead of SAC scheme is estimated to be less than 1% of overall power consumption.

V. CONCLUSION

The SAC scheme is applied to SRAM and its test chip is fabricated and measured. SAC uses an active control of the operation

conditions to overcome uncertainties of high-density SRAM. In the SAC scheme, on-chip sensors like an on-chip timer, temperature sensor, substrate noise detector, and leakage current monitor are used. An internal V_{dd} controller, substrate noise suppressor, and negative voltage generator are used as the control blocks. The test SRAM is fabricated in an 80-nm double stacked cell technology. The test results show that by using SAC the average power consumption is reduced by 9% from 15.9 to 14.4 mW, and the standard deviation decreases by 58% from 2.6 to 1.1 mW. Also, speed improvement is obtained by preset control margin of the on-chip timer. This work demonstrates that the sensing, analysis, and control scheme is very useful to obtain high yield in memory products like SRAM.

REFERENCES

[1] A. Kotabe et al., "A 0.13-μm, 0.78-μm^2 low-power four-transistor SRAM cell with a vertically stacked polysilicon MOS and a dual-word-voltage scheme," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2004, pp. 60–63.

[2] K. Osada, K. Yamaguchi, Y. Saitoh, and T. Kawahara, "SRAM immunity to cosmic-ray-induced multierrors based on analysis of induced parasitic bipolar effect," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 827–833, May 2004.

[3] S. Jung et al., "Highly area efficient and cost effective double stacked S^3 (stacked single-crystal Si) peripheral CMOS SSTFT and SRAM cell technology for 512 Mbit density SRAM," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2004, pp. 265–268.

[4] T. Burd, T. Pering, A. Stratakos, and R. Brodersen, "A dynamic voltage scaled microprocessor system," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1571–1580, Nov. 2000.

[5] R. Jejurikar and R. Gupta, "Dynamic voltage scaling for systemwide energy minimization in real-time embedded systems," in *Proc. IEEE Int. Symp. Low Power Electronics and Design (ISLPED)*, Aug. 2004, pp. 78–81.

[6] M. Nakai et al., "Dynamic voltage and frequency management for a low-power embedded microprocessor," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 28–35, Jan. 2005.

[7] S. Akui et al., "Dynamic voltage and frequency management for a low-power embedded microprocessor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2004, vol. 47, pp. 64–65.

[8] Samsung, SRAM Products [Online]. Available: http://www.samsung.com/Products/Semicon-ductor/SRAM/index.htm

[9] J. Sim et al., "A 1.8-V 128-Mb mobile DRAM with double boosting pump, hybrid current sense amplifier, and dual-referenced adjustment scheme for temperature sensor," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 631–640, Apr. 2003.

[10] K. Makie-Fukuda et al., "An on-chip active decoupling circuit to suppress crosstalk in deep-submicron CMOS mixed-signal SoCs," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 67–79, Jan. 2005.

[11] B. Owens et al., "Simulation and measurement of supply and substrate noise in mixed-signal ICs," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 382–391, Feb. 2005.

[12] M. Peng and H. Lee, "Study of substrate noise and techniques for minimization," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2080–2086, Nov. 2004.

[13] Y. Ye, M. Khellah, D. Somasekhar, A. Farhang, and V. De, "A 6-GHz 16-kB L1 cache in a 100-nm dual-Vt technology using a bitline leakage reduction (BLR) technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 839–842, May 2003.

[14] C. Wang, P. Lee, and K. Chen, "An SRAM design using dual threshold voltage transistors and low-power quenchers," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1712–1720, Oct. 2003.

[15] A. Agarwal, H. Li, and K. Roy, "A single-Vt low-leakage gated-ground cache for deep submicron," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 319–328, Feb. 2003.

[16] K. Nii et al., "A 90-nm low-power 32-kB embedded SRAM with gate leakage suppression circuit for mobile applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 684–693, Apr. 2004.

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